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CLAIMS 1-18 (CANCELLED)

19. A method of forming a vertical polymer transistor structure, said method comprising:

depositing a first conductive layer on a substrate;

patterning an etch stop strip over said first conductive layer;

depositing a semiconductor body layer over said first conductive layer;

depositing a second conductive layer over said semiconductor body layer, wherein said first conductive layer, said semiconductor body layer, and said second conductive layer comprise a laminated stack;

patterning said laminated stack to create a laminated structure, wherein said etch stop strip protects said first conductive layer during said patterning of said laminated stack;

removing at least a portion of said etch stop strip to expose said first conductive layer; and

forming contacts to said first conductive layer and said second conductive layer.

20. The method in claim 19, further comprising before said removing of said etch stop strip, forming sidewall spacers adjacent sides of said laminated structure, wherein said etch stop strip protects said first conductive polymer layer during said forming of said sidewall spacers.

21. The method in claim 19, wherein said patterning of said etch stop strip positions said etch stop strip at an outer edge of said semiconductor body layer.

22. The method in claim 19 wherein said patterning of said etch stop strip positions said etch stop strip on only one side of said vertical polymer of transistor structure.

23. The method in claim 19, wherein said source contact is on an opposite side of said laminated stack from said drain contact.

24. A method of forming a vertical polymer transistor structure, said method comprising:

depositing a first conductive layer on a substrate;

patterning an etch stop strip over said first conductive layer;

depositing a semiconductor body layer over said first conductive layer;

depositing a second conductive layer over said semiconductor body layer, wherein said first conductive layer, said semiconductor body layer, and said second conductive layer comprise a laminated stack;

patterning said laminated stack to create a first laminated structure and filler structures adjacent said first laminated structure;

patterning said semiconductor body layer and said second conductor layer of said first laminated structure to create a second laminated structure, wherein said etch stop strip protects said first conductive layer during said patterning of said first laminated structure;

removing at least a portion of said etch stop strip to expose said first conductive layer; and

forming contacts to said first conductive layer and said second conductive layer over said filler structures.

25. The method in claim 24, wherein said filler structures support said source contact and said drain contact.

26. The method in claim 24, further comprising before said removing of said etch stop strip, forming sidewall spacers adjacent sides of said laminated structure, wherein said etch stop strip protects said first conductive polymer layer during said forming of said sidewall spacers.

27. The method in claim 24, wherein said patterning of said etch stop strip positions said etch stop strip at an outer edge of said semiconductor body layer.

28. The method in claim 24, wherein said patterning of said etch stop strip positions said etch stop strip on only one side of said vertical polymer of transistor structure.

29. The method in claim 24, wherein said source contact is on an opposite side of said laminated stack from said drain contact.